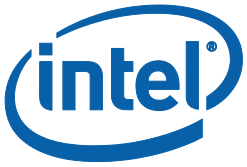


Intel® Thunderbolt Release Notes For Burnside Bridge A-Step

Release Notes - NDA

May 2019

Revision 28.0

Intel Confidential

Legal Disclaimer

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an order number and are referenced in this document, or other Intel literature, may be obtained by calling 1-800-548-4725, or go to:
http://www.intel.com/design/literature.htm

This document contains information on products in the design phase of development.

Intel, the Intel logo, Thunderbolt and the Thunderbolt are trademarks of Intel Corporation in the U.S. and/or other countries.

*Other names and brands may be claimed as the property of others.

Audience

This document intended for use by OEM software developers, test and validation engineers, and system integrators.

Contents

Revision History

Revision Number	Description	Revision Date
1.0	Initial Release for Burnside Bridge A0 step	April 2018
2.0	Engineering release for Burnside Bridge Rev 2.0	May 2018
3.6	ICL Pre-Alpha Burnside Bridge FW Rev 3.6	August 2018
4.3	Engineering release for Burnside Bridge Rev 4.3	August 2018
12.0	Initial Release for Burnside Bridge A1 step	September 2018
13.0	Engineering release for Burnside Bridge Rev 13.0	October 2018
14.0	Engineering release for Burnside Bridge Rev 14.0	October 2018
15.0	Engineering release for Burnside Bridge Rev 15.0	November 2018
16.0	Engineering release for Burnside Bridge Rev 16.0	07 January 2019
17.0	Engineering release for Burnside Bridge Rev 17.0	14 January 2019
18.0	Engineering release for Burnside Bridge Rev 18.0	24 January 2019
19.0	Engineering release for Burnside Bridge Rev 19.0	26 February 2019
20.0	Engineering release for Burnside Bridge Rev 20.0	8 March 2019
21.0	Engineering release for Burnside Bridge Rev 21.0	14 March 2019
22.0	Engineering release for Burnside Bridge Rev 22.0	21 March 2019
23.0	Engineering release for Burnside Bridge Rev 23.0	17 April 2019
24.0	Engineering release for Burnside Bridge Rev 24.0	28 April 2019
25.0	Engineering release for Burnside Bridge Rev 25.0	7 May 2019
26.0	Engineering release for Burnside Bridge Rev 26.0	14 May 2019
28.0	Engineering release for Burnside Bridge Rev 28.0	20 May 2019

1 Introduction

1.1 Scope of Document

This document provides component-level details of the downloaded release and the contents of each folder in the release.

1.2 Acronyms

Term	Description
TBT	Thunderbolt
HR	Host Router
EP	End Point
AIC	Add-In Card
PR	Port Ridge (Thunderbolt)
FR	Falcon Ridge (Thunderbolt 2)
AR	Alpine Ridge (Thunderbolt 3)
TR	Titan Ridge (Thunderbolt 3)
DP	Display Port
CM	Connection Manager
LC	Link Controller
HDCP	High-bandwidth Digital Content Protection
DB	Delta Bridge – TBT Retimer
BB	Burnside Bridge – TBT Retimer

1.3 Naming Convention:

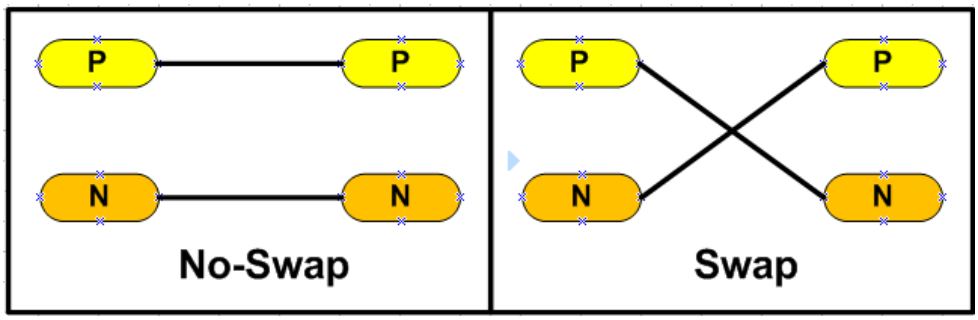
<project name>_<mode>_<Si stepping>_<image rev>.bin

For example
- <project name>:
  - LR, PR, AR, TR, etc.
- <mode>:
  - OB = Onboard

BB_CDR_A0_Rev10.bin – Burnside Bridge A0 stepping Revision 10

1.4 Lane N/P Swap configuration

Note: Each revision might have different instructions on how to control board-dependent channels lanes N/P swap configuration.



2 Release Summary

This document covers Intel® Thunderbolt Firmware for the Burnside Bridge. Starting version 12.0 same NVM binary will be used for both Burnside Bridge A0 and Burnside Bridge A1.

2.1 Release Overview

The release can be downloaded from ***Intel VIP*** (https://platformsw.intel.com/).

Note: Please use ***Thunderbolt Retimer Tool*** latest version **(Doc ID#: 597797)** from ***My Intel*** to configure retimer firmware correctly.

Note: A username and password are required to access the website and to log in. The user must have an account created for access.

3 Features Supported

Supported = ✓ Limited Support = ⚠ Not Supported = ✘

Technology	Support
Thunderbolt Link 20/40G	✓
Thunderbolt Link Power Management (CLx)	✓
SMBUS	✓
DisplayPort	✓
USB 3.1 Gen2/1	✓
Sx	✓
Wake	✓
Firmware update – TBT system	✓
Firmware update – Non-TBT system	×

3.1 Best Known Configuration

For the latest client-based platforms Best Known Configuration (BKC), please contact your platform CE.

4 New Features–RCRs

RCR #	Title	Change Info	Status

5 Issue Status Definitions

This document provides sightings and bugs report for Intel® Thunderbolt Burnside Bridge SKUs. At the time of a milestone release, this report will be distributed with the Intel® TBT Release and will provide information on new issues and the status of old issues (replacing the Release Notes document).

Closed Issues: This category will only display closed issues within the current Intel® TBT release. After each release, old issues will be dropped down to the "Archive" section and then new closed issues will take its place back up top for the next release. If an issue is posted in this section, it will indicate that the issue has been verified and fixed within the one that is being released.

Known Issues: This category will display all Known Issues since the initial release and will remain in this section until fixed or noted otherwise. "Known Issues" are still under investigation and may or may not be root caused.

Archive – Fixes in Previous releases: This category will display all closed issues that were closed in their respected release#. This section will serve as a history of fixed issues.

Sightings listed in this document apply to the Thunderbolt™ Burnside Bridge SKUs unless noted otherwise in this document or in the sightings tracking systems.

5.1 Fixed Issues in This Release

Issue Closed in Release #	Title	Details
28	**Disable Tx Compliance mode**	**Sighting #:** 5324431 **Affected Component:** USB **Impact:** Disables Tx Compliance mode by default.

5.2 Known Issues–To Date

Issue Found in Release #	Title	Details
28	**SMBUS/flash buffer conflict**	**Sighting #:** 1306484849 **Affected Component:** LC **Impact:** SMBUS/flash buffer conflict causes authentication failures when running capsule update cycles on non-TBT systems

5.3 Archive–Fixes in Previous Releases

Issue Fixed in Release #	Title	Details
26	**Workaround the AUX NP for BBR**	**Sighting #:** N/A **Affected Component:** DP **Impact:** Added a configuration bit for workaround the AUX NP bug in BBR.
26	**TBT connection while system is in Sx**	**Sighting #:** 5324427, 2207488704 **Affected Component:** LC **Impact:** Retimer does not wake up when the system exits Sx/G3 causing enumeration failure on G3 **Fix:** Fixed the TBT connection issue while the system is in Sx.
25	**Display is not enumerating when display is hot plugged behind MFD dongle**	**Sighting #:** 1607085771 **Affected Component:** DP **Impact:** Display is not detecting while hot plugging display to MST hub (TypeC-DP Hub). **Fix:** Removing SRC_DIS_REQ from LC only in BBR upon sink_count =0
25	**Enabled compliance**	**Sighting #:** 5324431 **Affected Component:** USB **Impact:** Enable the compliance by default.
24	**USB3 Gen1 devices are downgraded to USB2**	**Sighting #:** 1306342513 **Affected Component:** PHY **Impact** USB3 Gen1 devices are downgraded to USB2 after S4/Warm Reset cycles.
23	**SMBUS enablement**	**Sighting #:** N/A **Affected Component:** LC **Impact:** Enable SMBUS for non-TBT SKU to support Retimer Capsule FW.
23	**Tx min LFPS**	**Sighting #:** N/A **Affected Component:** PHY **Impact:** Incorrect CLx exit handling **Fix:** In CIO mode, increase Tx min LFPS to 7 for correct CLx exit handling.
23	**Reed-Solomon(RS) errors on DMA traffic to EP**	**Sighting #:** N/A **Affected Component:** PHY **Impact:** RS errors on DMA traffic to EP **Fix:** Failure was observed in case of remote electrical idle from toggling TxPLL charge pump, This fixes RS errors on DMA traffic to EP allowing FW to handle the rapid CL0s transitions.
22	**LTTPR non-transparent mode**	**Sighting #:** N/A **Affected Component:** DP **Impact:** LTTPR should not edit downstream capabilities, in LTTPR non-transparent mode, on DPCD 0x00000 area.
22	**Port S3 USB Mode Entry**	**Sighting #:** 5324413 **Affected Component:** LC **Impact:** Allow the port FSM to enter USB connection in Sx state but prevent the system to wake up from S3/S4 state on Retimer Ports.

Issue Fixed in Release #	Title	Details
22	**Disable IECS flash access**	**Sighting #:** N/A **Affected Component:** LC **Impact:** Add config to disable flash access IECS operations.
21	**Update the TPS capabilities**	**Sighting #:** 5324406 **Affected Component:** DP **Impact:** Display does not wake up after switching 2 monitors DP cables **Fix:** Update TPS capabilities upon every access to DPCD Cap.
21	**LTTPR mode**	**Sighting #:** 5324416 **Affected Component:** DP **Impact:** DP TX link quality fails when using non-LTTPR and LTTPR-transparent mode **Fix:** Update CM with the right bandwidth upon DPRX-READ-CAP-BIT also in LTTPR mode.
21	**PHY TX CTS**	**Sighting #:** N/A **Affected Component:** DP **Impact:** Adjustment to make PHY TX CTS more robust (when using different GPUs).
21	**Compliance mode changes**	**Sighting #:** 5324334 **Affected Component:** LC **Impact:** New compliance workaround(WA) caused false entries to compliance mode **Fix:** Revert to old compliance WA.
20	**TPS capabilities**	**Sighting #:** N/A **Affected Component:** DP **Fix:** Fix for issue where TypeC to DP dongle is connected to BBR, and BBR is using wrong TPS when switching monitor setting from DP1.2 to DP1.1.
20	**U1 tx lfps**	**Sighting #:** N/A **Affected Component:** USB **Impact:** Changed min U1 tx lfps duration to 1.6us to solve interop issue with certain 3rd party retimers and to solve compliance pre-cert issue with ICL
19	**PHY TX CTS**	**Sighting #:** N/A **Affected Component:** DP **Impact:** Support for test request when AUX request comes in a burst (reading of 0x201 + some more DPCD registers).
19	**LTTPR**	**Sighting #:** N/A **Affected Component:** DP **Impact:** Return ACK instead of NACK on PHY_REPEATER_MODE if the first transaction was writing LTTPR Transparent mode (F0003, 0x55).
18	**Non-secure fw**	**Sighting #:** 2206263348 **Affected Component:** LC **Fix:** fix authentication regression introduced in previous update.

Issue Fixed in Release #	Title	Details
18	**wake from TBT**	**Sighting #:** 5324396 **Affected Component:** LC **Fix:** fix issue with wake from TBT caused by previous w/a for no-wake cases.
18	**TBT connection while system is in Sx**	**Sighting #:** 5324397 **Affected Component:** LC **Fix:** fix issue with TBT connection while system is in Sx
17	**CIO CLx Exit**	**Sighting #:** 1606905420 **Affected Component:** TBT **Impact:** Link failures on CLx exit (affecting functionality on Sx exit and unplug/plug) as a result of false SSC indication. **Fix:** SSC indication and link training time adjustment.
16	**Wake from Sx on TBT disconnect**	**Sighting #:** 1305928535 **Affected Component:** TBT **Impact:** Sx wakes up the system on disconnect event. **Fix:** Retimer masks the disconnect event from LSx to allow disable of the wake capability from the LSx (by PMC).
16	**Warm reset while in U3**	**Sighting #:** 5324374 **Affected Component:** USB **Impact:** After placing a DUT link into U3, and then issuing a port reset, the PUT does not transmit a Warm Reset LFPS. **Fix:** The issue is fixed with the retimer forwarding warm reset in U3 such that the affected flows exit from S4/S5 while device is connected. Also, the fix allows port to pass TD 7.35 in compliance test suite.
16	**Entry Tx to compliance mode**	**Sighting #:** 5324360, 5324334 **Affected Component:** USB **Fix:** Fixes the issue with USB entering Tx compliance mode. Now entry is in accordance to specification.
15	**Rx detect interval reduced**	**Sighting #:** N/A **Affected Component:** USB **Fix:** Reduced Rx detect intervals to 3ms. This prevents potential issue of fallback to USB2.0 during enumeration on long timing topologies.
15	**LFPS detection sensitivity**	**Sighting #:** 5324364 **Affected Component:** USB **Impact:** Link failed to return to U0 after few iterations of U2 to U1 flow. It was found that retimer did not recognize ping.lfps from device side in U1 state, thus the link failed to detect. **Fix:** LFPS detection sensitivity was increased to fix this issue.
15	**Power wait time**	**Sighting #:** 1408268442 **Affected Component:** USB **Impact:** Enhanced super speed device initiated remote wakeup and the host ACK'ed the request. However, the link never transitioned to U0 (always stayed in U3). **Fix:** The issue is fixed by increasing the power-off wait period to be 128ms. This prevents retimer from going back to U3 low power between exit attempts (the interval between them is 100ms).

Issue Fixed in Release #	Title	Details
14	**Tapex Card link training fails if FORCE POWER to retimer is ASSERTED when CLx is enable**	**Sighting #:** 1407950200 **Affected Component:** PHY **Impact:** Fix re-plug corner-cases when forced-power mode set to intel retimer fails while CLx is enabled.
14	**USB 3 Devices re-enumerates after wake from S4**	**Sighting :** 1604822704 **Affected Component:** USB **Impact:** Sporadic failures with some USB 3.0 devices that continuously re-enumerate after wake from S4.
14	**Burst register write**	**Sighting #:** N/A **Affected Component:** DP **Fix:** Increased robustness to burst write of BW/LANEs/TPS all together.
14	**Auto-wake is observed during Sx with TBT 2 devices**	**Sighting #:** 1506748870 **Affected Component:** LC **Impact:** Auto-wake was observed during Sx with tunneled and type-C displays. **Fix:** The issue is fixed by not sending LT fall during Sx entry when legacy device is connected.
14	**Tapex Card link training fails if FORCE POWER to retimer is ASSERTED when CLx is disabled**	**Sighting #:** 1407950200 **Affected Component:** PHY **Impact:** When retimer *FORCE_POWER* was *ASSERTED*, Tapex card link training failed. Fix re-plug corner-cases when forced-power mode set to intel retimer.
13	**Verify Sx exit**	**Sighting #:** 5324321 **Affected Component:** LC **Impact:** Added logic to verify Sx exit connection state versus Sx entry state and to clear relevant indications that might otherwise not have got cleared.
13	***IECS_DATA* after authentication availability**	**Sighting #:** 5324301 **Affected Component:** LC **Impact:** Make sure authentication error code is available to SW in *IECS_DATA* after authentication failed by avoiding it being cleared on INIT state.
13	**Remove delay disconnect**	**Sighting #:** 5324298 **Affected Component:** LC **Impact:** Do not delay disconnect if *LRoff* is received and the port is not in *TBT_HIGH_SPEED*.
13	**Disconnect ports on *LRoff* receive**	**Sighting #:** 5324298 **Affected Component:** LC **Impact:** Disconnect both ports even if *LRoff* is received from one side only.
13	**Force reset for USB retimer *LTSSM***	**Sighting #:** 5324292 **Affected Component:** LC **Impact:** Force reset the USB retimer *LTSSM* while asserting *power_ack* to allow PLL clock to trickle through the design.

Issue Fixed in Release #	Title	Details
13	***Rx_Detect* duration**	**Sighting #:** N/A **Affected Component:** USB **Impact:** Change *Rx_Detect* duration as per EV requirements.
13	**Sporadic display failures during hot plug/cold boot event**	**Affected Component:** DP **Impact:** Sporadic display blackout seen with USB-C to USB- C or USB-C to DP during hot plug/unplug and cold boot scenarios.
12	**DP voltage swing change during link training**	**Sighting #:** N/A **Affected Component:** DP **Impact:** DP-IN won't reach to maximum voltage swing during CR phase unless last attempt or DP-OUT finished link training.
12	**DEFER mismatch between DP IN and DP OUT**	**Sighting #:** N/A **Affected Component:** DP **Impact:** DP-OUT won't take into account defers from DPRX for the total number of allowed retries.
12	**USB U3 exit delay**	**Sighting #:** 5324292 **Affected Component:** LC **Impact:** On U3 exit, delay retimer ***power_ack*** until PHY port ***init_done*** rise on both ports.
12	**Speed up USB connection**	**Sighting #:** N/A **Affected Component:** LC **Impact:** Allow USB retimer's EE2TARs load to complete before FW load to speed up USB connection.
12	**New spec compliance alignment**	**Sighting #:** N/A **Affected Component:** LC **Impact:** Add support for 'GNSS' (get NVM sector size) mailbox command and remove power cycle command support.
12	**NVM update vulnerability**	**Sighting #:** N/A **Affected Component:** LC **Impact:** Fixed vulnerability due to lack of extended skiplist pointer handling during the update.
12	**Secure update**	**Sighting #:** N/A **Affected Component:** LC **Impact:** Secure update –fix bonded UUID flow and allow key change/security revision change when skip authentication is set.
12	**DP low power modes**	**Sighting #:** N/A **Affected Component:** LC **Impact:** Enable DP low power modes by default.
12	**DP mode entrance**	**Sighting #:** N/A **Affected Component:** LC **Impact:** Enter DP modes regardless of HPD state (low or high).
4.3	**DP Voltage Swing Pre-Emphasis**	**Sighting #:** N/A **Affected Component:** DP **Impact:** DP SNK will change the requested VSPE to overcome source that gives up on Link Training before 5th attempt.

Issue Fixed in Release #	Title	Details
4.3	**DP Link Layer compliance**	**Sighting #:** N/A **Affected Component:** DP **Impact:** Fix for LL compliance to reflect clock recovery bits correctly during clock recovery phase.
4.3	**DP link training**	**Sighting #:** N/A **Affected Component:** DP **Impact:** Enabled link training in transparent mode (after reading 0xF0000 but before going into LTTPR mode).
4.3	**DP modes entry**	**Sighting #:** N/A **Affected Component:** LC **Impact:** Enter DP modes regardless of HPD state.
4.3	**DP source PU**	**Sighting #:** N/A **Affected Component:** LC **Impact:** Expose source PU only after DP domain is powered-up.
4.3	**USB compliance mode entry**	**Sighting #:** N/A **Affected Component:** USB **Impact:** Disable path to compliance mode for a non-compliant device.
4.3	**USB LFPS**	**Sighting #:** N/A **Affected Component:** USB **Impact:** Reduce LFPS detect minimum period to 9 for detecting LFPS on the lower threshold.
4.3	**USB SKP in Gen1**	**Sighting #:** N/A **Affected Component:** USB **Impact:** Disable adding SKP's during logical idle in gen1 USB devices.
3.6	**DP-AUX error handling by DP-Input**	**Sighting #:** N/A **Affected Component:** DP **Impact:** DP-AUX not responding some messages when GPU is interleaving AUX requests frequently.
3.6	**DP-OUT trains with TPS4 on limited capability scenario**	**Sighting #:** N/A **Affected Component:** DP **Impact:** Issue on wake flow where GPU does not read TPS capabilities DPCD registers, thus DP-OUT lacking DPRX's TPS capabilities info.
3.6	**DP LTTPR disabled when configured from NVM**	**Sighting #:** N/A **Affected Component:** DP **Impact:** DPCD addresses 0xF000-0xF000F set to be internal with value of 0x0 when LTTPR support is disabled in NVM.
3.6	**DP Set_Power (0x600) AUX set to be external**	**Sighting #:** N/A **Affected Component:** DP **Impact:** *Set_Power* configuration message will be sent upon write to update device ridge. This was done to avoid corner cases where DP-IN ACKs GPU on 0x600 but the 0x600 transaction initiated by DP-OUT deferred for long time by the monitor.

Issue Fixed in Release #	Title	Details
3.6	**Fallback mechanism support for three redrivers**	**Sighting #:** N/A **Affected Component:** DP **Impact:** On transparent mode, added some defers from DP-IN during Link Training – Clock Recovery phase in case DP-OUT hasn't reported CR_DONE on the next hop. This is done to overcome case where it takes few attempts for the monitor to reach CR_DONE.
3.6	**Tune TX PLL flow**	**Sighting #:** N/A **Affected Component:** DP **Impact:** SSC configuration fix on DP-OUT.
3.6	**BBR-A0 100MHz oscillator**	**Sighting #:** N/A **Affected Component:** LC **Impact:** Regardless of NVM configuration, keep 100MHz oscillator enabled for BBR-A0 only.
3.6	**Block SVR domain power**	**Sighting #:** 5324191 **Affected Component:** LC **Impact:** Never request to power-up PC power domain, or else, attempted to be turned on, it blocks SVR domain power off.
3.6	**USB warm reset**	**Sighting #:** N/A **Affected Component:** USB **Impact:** Disable fast warm reset in non-Ux states.
2	**DisplayPort –** **Three Redrivers SSC**	**Sighting #:** **Affected Component:** DP **Impact:** Added fallback mechanism and SSC in three redriver configurations.
2	**DP compliance alignment**	**Sighting #:** **Affected Component:** DP **Impact:** Include additional AUX reads in order to align certain GPUs to DP spec. **Workaround:** Disconnect TBT device and perform reset/Sx.
2	**DP automatic test flow**	**Sighting #:** **Affected Component:** DP **Impact:** Require ***automatic_test_request*** as condition for test flow.
2	**Undo PLL reset flow for DP**	**Sighting #:** **Affected Component:** DP **Impact:** Reset PLL only on power down or link initialization.
2	**HDMI adapter malfunction**	**Sighting #:** **Affected Component:** DP **Impact:** Enable certain HDMI adapters to support LTTPR.
2	**Flash access before force power**	**Sighting #:** **Affected Component:** LC **Impact:** Assure flash is idle before forcing power cycle.
2	**LFPS ON-period**	**Sighting #:** **Affected Component:** LC **Impact:** Change LFPS ON-period to avoid detection sensitivity.

Issue Fixed in Release #	Title	Details
2	**N/P Swap**	**Sighting #:** **Affected Component:** PHY **Impact:** Corrected data handling affecting certain N/P configurations functionality.